IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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MANUFACTURING OF DISLOCATION FREE STRESSED CHANNELS IN BULK SILICON AND SOI CMOS DEVICES BY GATE STRESS ENGINEERING WITH

SiGe AND/OR Si:C

Confirmation No: 3238

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RESPONSE UNDER 37 C.F.R. § 1.116

Sir:

In response to the Final Rejection dated June 26, 2007, Applicants submit the following remarks for entry of record in the above-identified patent application.

Amendments to the Claims are provided in the Listing of Claims beginning on page 2 of this paper.

Remarks begin on page 9 of this paper.

CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this correspondence is being deposited with the United States Patent & Trademark Office via Electronic Filing through the United States Patent and Trademark Office e-business website, on August 27, 2007.

Dated: August 27, 2007